Ultra-Low-Coercive-Voltage Scaled $BaTiO_3$ Ferroelectric p-Bits for Probabilistic Computing

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Probabilistic bits (p-bits) are stochastic binary units that fluctuate between +1 and –1 with a tunable probability, offering a hardware foundation for invertible logic, probabilistic inference, and generative models. Hardware implementations of p-bits have traditionally relied on unstable nanomagnets or thermal noise sources to induce randomness [1,2]. While effective, these approaches face integration and scaling challenges, particularly in achieving compatibility with standard CMOS processes. To address this, we introduce a new class of ferroelectric p-bits based on a scaled 20 nm $BaTiO_3$ (BTO) capacitor with ultra-low coercive voltage, integrated in a 1T–1F configuration where the transistor provides the noise source.

The BTO capacitor exhibits robust ferroelectric switching, confirmed by well-saturated polarization-voltage loops and distinct Positive-Up-Negative-Down (PUND) characteristics. The extremely low coercive threshold makes the polarization state highly susceptible to small-amplitude fluctuations, allowing intrinsic temporal voltage noise from a CMOS transistor to directly perturb the ferroelectric free-energy landscape and drive stochastic state transitions.

To induce stochasticity, we exploit transistor noise as characterized by Lu et al. [3], superimposing it on the bias applied to the ferroelectric capacitor. Under these conditions, the device exhibits a voltage-dependent switching probability curve with a sigmoidal transfer characteristic, consistent with thermally activated polarization reversal statistics in ferroelectrics. We experimentally demonstrate that at zero bias, the polarization output exhibits an approximately symmetric (~ 50/50) distribution between the two stable states, while small positive or negative biases skew the state occupancy (e.g., 90/10 or 97/3), with the degree of asymmetry tunable by the noise amplitude. These output distributions correspond to controllable variations in the free energy profile of the ferroelectric under noise-driven operation.

This work introduces ferroelectric materials as a new medium for p-bit hardware and establishes a CMOS-compatible, scalable, and low-energy approach for probabilistic computing. The 1T-1F ferroelectric p-bit enables future architectures in invertible logic, hardware Bayesian networks, and neuromorphic systems.

References

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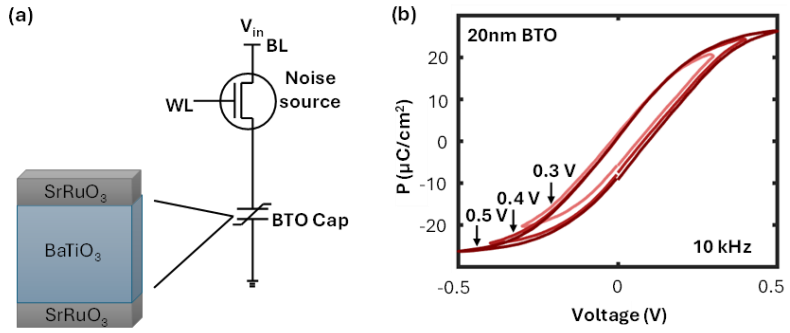

FIG. 1. Baseline characterization of the $BaTiO_3$ device. (a) Schematic of the proposed p-bit, a 1T-1F cell with $BaTiO_3$ capacitor connected to a transistor which acts as a noise source while offering a readout mechanism for the ferroelectric capacitor. (b) P-V hysteresis loop at a frequency of 10 kHz.

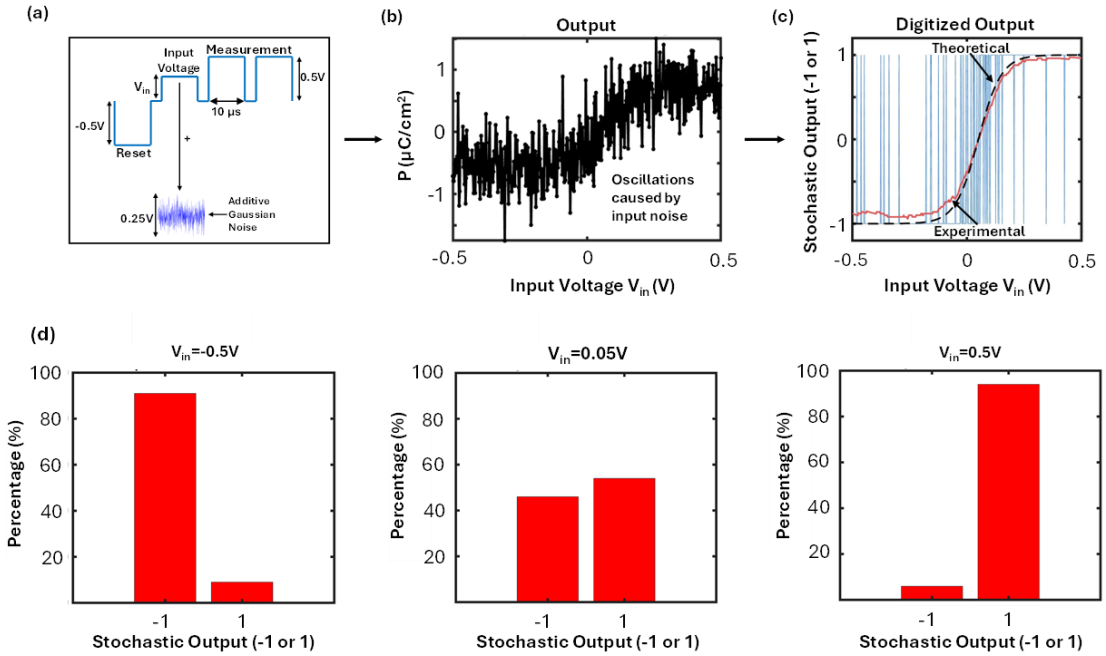

FIG. 2. Input signal and resulting output graphs for PUND measurements with simulated voltage noise. (a) Plot of a generic PUND waveform with additive Gaussian noise. (b) Resulting output from input (a) measuring polarization as a function of switching voltage. (c) Binary digitized output from (b) plotted with a moving average and fitted tanh(x) function. (d) Output distributions at each voltage level across 100 repeated trials.